UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

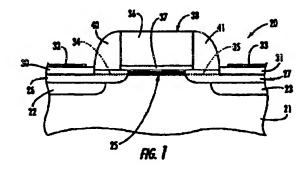
PATENT NO. : 6,891,188 B2 Page 1 of 2

APPLICATION NO.: 10/717374
DATED: May 15, 2005
INVENTOR(S): Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Drawings Delete: FIG. 1

Insert: New FIG. 1



Column 1, Line 42

Delete: "on a binary" Insert: --on binary--

Column 1, Line 66 Delete: "in a silicon"

Insert: --in silicon--

Column 1, Line 67 Delete: "electromuminescence"

Insert: --electroluminescence--

Column 3, Line 4 Delete "as may"

Insert: --as may be--

Column 5, Line 11 Delete: "gate 35"

Insert: --gate 38--

Column 5, Line 60 Delete: "gate 35"

Insert: --gate 38--

Column 7, Line 63 Delete: "from the both"

Insert: --from both--

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PATENT NO. : 6,891,188 B2 APPLICATION NO.: 10/717374

INVENTOR(S)

: Mears et al.

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> It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9, Lines 44-46 Delete: "In other processes and devices the structures of the

present invention may be formed on a portion of a wafer or

Page 2 of 2

across substantially all of a wafer."

Column 9, Line 59 Delete: "also formed"

Insert: --also be formed--

Signed and Sealed this

Twenty-sixth Day of September, 2006

JON W. DUDAS Director of the United States Patent and Trademark Office